Effective Detection Mechanism of Missing Output Clock Pulse of an OCXO used for 5G Application

Kamalkumar S
R and D
Rakon India Pvt. Ltd.
Bangalore, India
Kamalkumar.s@rakon.com

Nalini CV
R and D
Rakon India Pvt. Ltd.
Bangalore, India
Nalini.cv@rakon.com

Chandrashekar M
R and D
Rakon India Pvt. Ltd.
Bangalore, India
Chandrashekar.mariyappa@rakon.com

Summary-Rapid evaluation of telecom technology over the last few years has forced OCXO design and manufacturing to technology. Especially 5G technology calls for stringent requirements, where OCXO plays a key role in 5G systems which defines time and synchronization operations.

Every pulse or clock output of OCXO is crucial to manage traffic in routers and 5G system. Missing clock pulse or cycle from OCXO due to malfunctioning of OCXO output buffer IC. Since each clock is in nSec depended on frequency, detection of missed pulse is highly difficult and cannot be simulated using soft tools before design and development, it is critical to identify the OCXOs with missing clock pulse failure nature before ship to customer.

The research article explains on the mechanism to screen the parts for the failure nature of missed clock pulse reported by customer, root cause for the failure and characterization of Output buffer IC of an OCXO. In order to avoid the faulty part reaching customer, developed customized test mechanism to screen the parts with failure nature.

Keywords— OCXO, Clock Pulse, I-V curve, missed clock,

I. INTRODUCTION

The OCXOs dwells a key role in Frequency controlled products to have best accuracy and high precision signal synchronization. Since the demand and requirements for the high stability OCXOs are increasing for high reliable with high quality and performance every clock pulse from OCXO is highly important and miss of a single pulse would lead to high damage at 5G application.

Missing OCXO output clock pulse is a random event occur at indefinite time interval for shorter duration and operates in good condition for rest of the time. No clock output during boot up at customer application causes error boot up issue. This issue is recoverable after several power cycle trials. The problem is repeated during resting of the board after few days of duration. It is highly difficult to estimate the occurrence duration of this failure at end application and it is huge cost to detect and replace faulty parts on end application board.

This type of failure reported by Customer cannot be simulated with any soft tools before design, develop and test.

II. METHODS/RESULTS

Customer Failure nature reproduced at manufacturing site as shown in Fig 1 and Fig 2 and developed customized test set up with a dedicated mechanism to detect missing clock pulse event as mentioned in Fig 3 and logic flow diagram in Fig 4

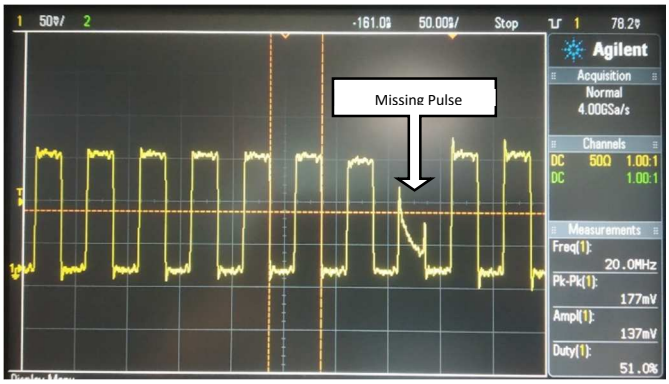

FIG 1 Detected missed clock pulse

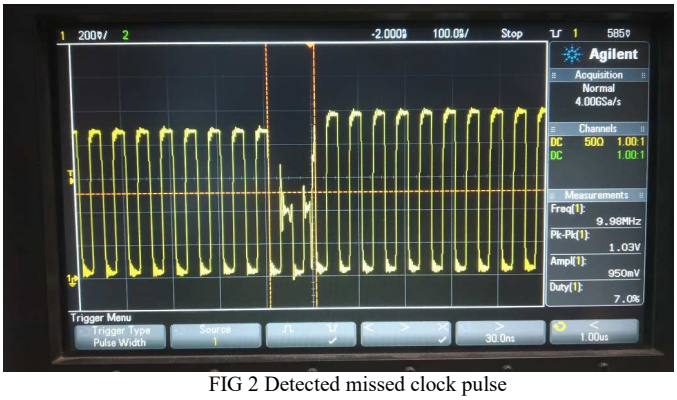

FIG 2 Detected missed clock pulse

OCXOs which were failed at customer application were taken for analysis and could reproduce the failure nature as shown in Fig 1 and Fig 2. Which clearly gives an information about high level of the signal was degraded to less than 50 % of its actual peak for few cycles. Reduced High level will be treated as no Clock at customer application.

Testing mechanism to detect failure signature

Identification of failure nature is highly challenging and measurement /capturing data at nSec intervals required highly sophisticated and advanced technology equipment's with high

storage memory. As an alternate approach, logic and mechanism implemented with in-house customized test setup and software as per flow chart Fig 4.

Prepare the test set up as shown in Fig 3, Power on the OCXO at 3.3V supply inside temperature chamber and set the temperature to 85Deg to make the OCXO to experience high temperature to accelerate failure condition. Measure and monitor output frequency and the wave form shape in oscilloscope continuously for 15 days with dedicated software designed for the application in interface with computer.

Software is prepared to detect any abnormalities and any major deviation in signal high level, low level, duty cycle, Rise time and fall time.

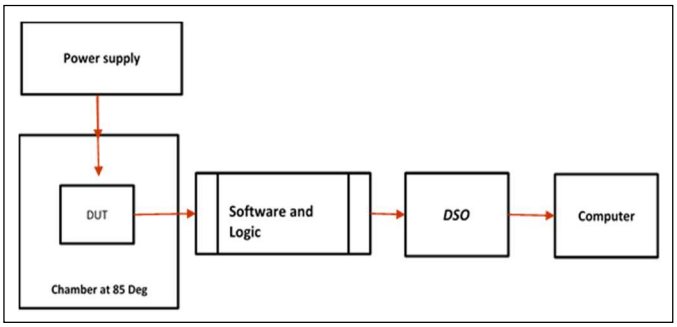

FIG 3 Block diagram for customized mechanism

Fig 4 shows the flow chart of the logic and mechanism followed to test and identify the OCXO that tend to behave abnormal at indefinite time intervals may be weeks of time or months. Missing clock is not a regular failure condition which will repeats frequently or at certain time intervals.

In order to capture failure condition such as missing pulse, utilized the feature of oscilloscope called “Trigger”. Trigger option, set the Pulse width trigger level with respect to one Cycle time duration, Example cycle duration for 10MHz signal is 100nSec, 50nSec for 20MHz 20nSec for 50MHz signal.

This option can be with positive pulse width or negative Pulse width. Here Positive Pulse width trigger used to identify the signal which is not in the defined limits with respect to Positive edge and successive negative Edge and for the Negative Pulse width trigger is used to identify the signal which is not in the defined limits with respect to Negative edge and successive Positive Edge.

One more option with Edge Trigger can be utilized to identify the failure condition with respect to Rise and Fall time variations. Oscilloscope used to generate an Event when the signal found out of defined specification, this event will be considered a missed pulse. Count of every event will get added and give information about number of times OCXO failed to produce good signal and time interval between failures.

If no event recorded till 15 days of test duration, then OCXO will be considered as good and Missing Pulse failure condition has detected.

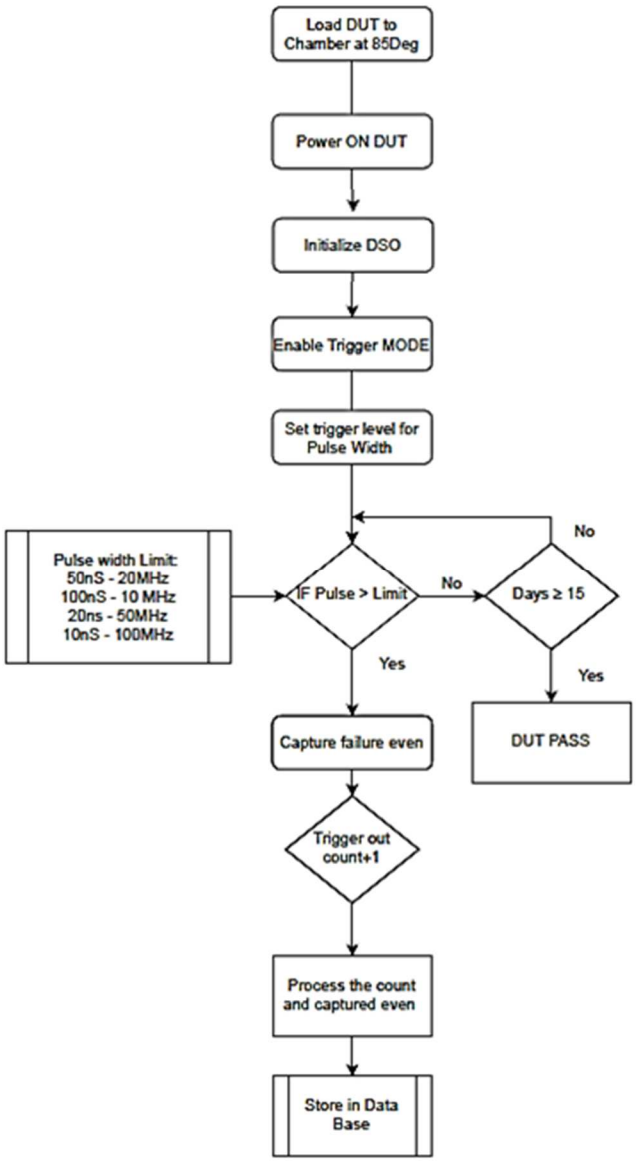

FIG 4 Logic diagram for customized mechanism

III. DISCUSSION/INTERPRETATION

The failure nature analyzed and identified with the help of customized test setup and the test mechanism is highly effective in accelerating the OCXO to detect the failure within 15Days if OCXO has any weakness.

Further analysis carried out to identify the root cause for the OCXO failure. OCXO was cut opened and probed for electrical signals and to characterize with respect to thermal and electrical performance of each sections, resulted in identified Output section of an OCXO has a weakness to produce good signal continuously, this we have identified by probing signal at input and output of Output section. Found Missing signal at output of Outputs section of OCXO even though there was a good signal at its input. Further analysis narrowed down to Output section and found Buffer IC which is used in output section has a

weakness to produce good signal continuously due to malfunction of output buffer IC at elevated temperatures.

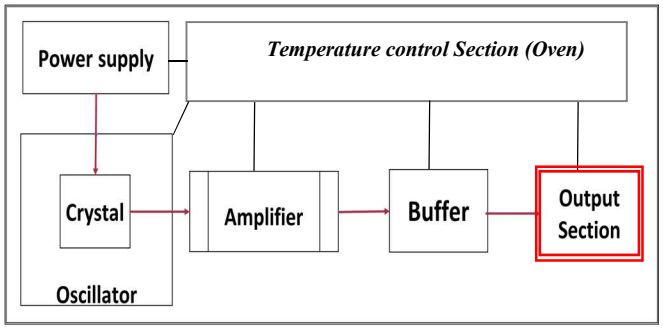

Fig 5 Block diagram of OCXO

Fig 5 shows Block diagram of an OCXO where quartz Crystal used to generate sustained oscillations with the help of supporting electronics and further signal will amplify to a required level with the help amplifier and buffer, the amplified sine signal will be converted to Square signal in Output section where logic Buffer plays an important role, signal processing and conversion will be done at Output section.

Output buffer IC characterized for different parameters and found abnormal random behavior at elevated temperature of 85°C. Good resistive I-V curve was observed at ambient temperature of 25°C, Open or abnormal I-V curve observed at hot temperature, as shown in FIG 6 and 7.

Output of Output buffer IC characterized for all pins and found output pin shows abnormal I-V curve at positive bias during high temperature (85deg) and found normal behavior at ambient temperature.

Resistance I-V measured done with respect each pin at ±5V supply and 4mA current source.[5]

Resentence measured at each PIN of Buffer IC and found the results as in Table 1

TABEL 1 MEASURED RESISTANCE AT EACH PIN WITH REFERENCE TO OTHER PINS AT AMBIENT TEMPERATURE

I-V curve Testing at Ambient temperature					
	Pin 1 (OE)	Pin 2 (A)	Pin 3 (GND)	Pin 4 (Y)	Pin 5 (Vcc)
Pin 1 (OE)		Good	Good	Good	Good
Pin 2 (A)	Good		Good	Good	Good
Pin 3 (GND)	Good	Good		Good	Good
Pin 4 (Y)	Good	Good	Good		Good
Pin 5 (Vcc)	Good	Good	Good	Good	

TABEL 1 represents the resistance measured at each PIN reference to other PINs and this shows results are good and No abnormalities Noticed at ambient Temperature.

TABEL 2 MEASURED RESISTANCE AT EACH PIN WITH REFERENCE TO OTHER PINS AT COLD -20DEG TEMPERATURE

I-V curve Testing at Cold (-20°C) temperature					
	Pin 1 (OE)	Pin 2 (A)	Pin 3 (GND)	Pin 4 (Y)	Pin 5 (Vcc)
Pin 1 (OE)		Resistive	Good	High resistance	High resistance
Pin 2 (A)	High resistance		Good	Good	Good
Pin 3 (GND)	Good	Good		Good	High resistance at
Pin 4 (Y)	High resistance	High resistance	Good		Good
Pin 5 (Vcc)	High resistance	High resistance	High resistance	Good	

TABEL 2 represents the resistance measured at each PIN reference to other PINs at -20Deg and this shows results with abnormalities high resistance. Buffer IC has some weakness at Cold temperature and which is reflected in terms of High resistance under bias condition.

TABEL 3 MEASURED RESISTANCE AT EACH PIN WITH REFERENCE TO OTHER PINS AT HIGH TEMPERATURE 85DEG

I-V curve Testing at Hot (85°C) temperature					
	Pin 1 (OE)	Pin 2 (A)	Pin 3 (GND)	Pin 4 (Y)	Pin 5 (Vcc)
Pin 1 (OE)		High resistance	Good	High resistance	High resistance
Pin 2 (A)	High resistance		Good	High resistance	High resistance
Pin 3 (GND)	Good	Good		High resistance	High resistance
Pin 4 (Y)	High resistance	High resistance	High resistance		High resistance
Pin 5 (Vcc)	High resistance	High resistance	High resistance	High resistance	

TABEL 3 represents the resistance measured at each PIN reference to other PINs at 85Deg and this shows results with abnormalities high resistance. Buffer IC has high weakness at High temperature, which is reflected in terms of High resistance under bias condition.

For more details refer Fig 6 to understand the behavior of Output buffer IC output PIN at different temperatures:
Behaved as per requirement under Room temperature condition. .*[5]*

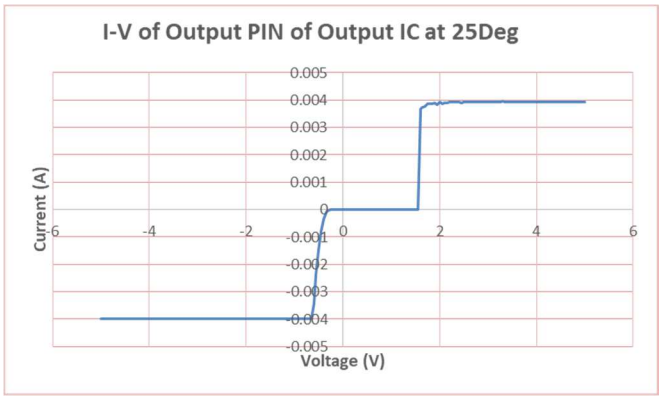

FIG 6 Output Buffer IC characterized for I-V at 25 Deg

Refer Fig 7 to understand the behavior of Output buffer IC output PIN at 85Deg temperatures:
Output Pin of Buffer IC behaved abnormal under elevated temperature condition. .*[5]*

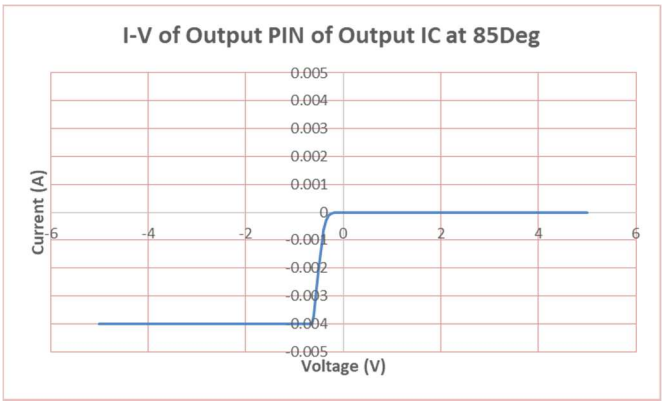

FIG 7 Output Buffer IC characterized for I-V at 85 Deg

Fig 8 shows the characterization of GND pin of OUTPUT Buffer IC with respect to Output Pin, this is the comparison between Buffer ICs from identified Good and failed OCXOs fro missing pulse failure condition. Failed OCXO Buffer IC behavior is abnormal at negative bias condition as shown in Table 3 at 85Deg temperature.

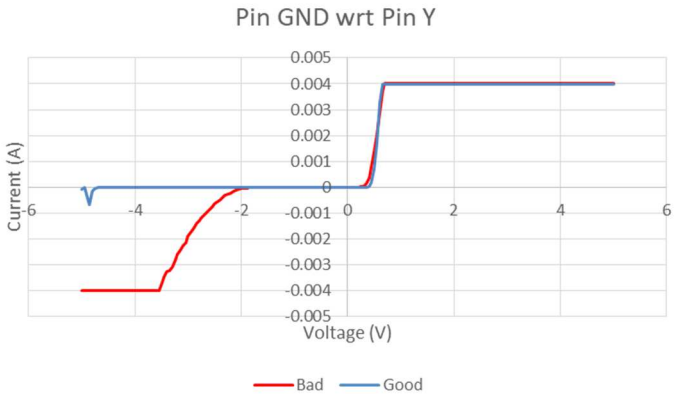

FIG 8 Output Buffer IC GND PIN characterized for I-V with respect to output PIN

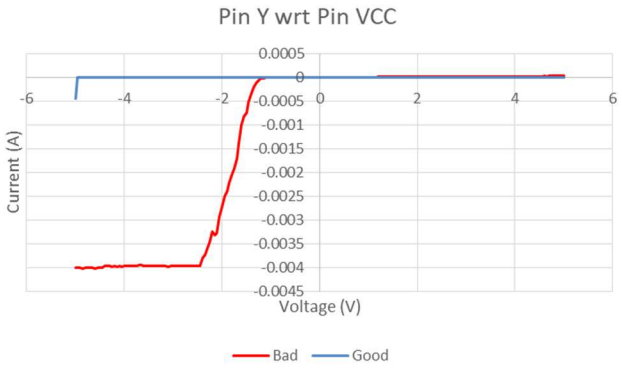

FIG 9 Output Buffer IC Output PIN characterized for I-V with respect to Vcc PIN

Fig 9 shows the characterization of OUTPUT pin of OUTPUT Buffer IC with respect to Vcc Pin, this is the comparison between Buffer ICs from identified Good and failed OCXOs fro missing pulse failure condition. Failed OCXO Buffer IC behavior is abnormal at negative bias condition as shown in Table 3 at 85Deg temperature.

Identified failed Buffer IC further analyzed for internal damages:

1. Fig 10 shows 2D X-ray inspection: Did not detect obvious wire anomaly on the sample.
2.

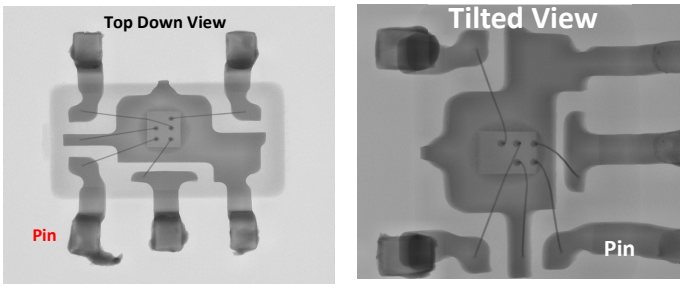

FIG 10 2D X-ray inspection of Output Buffer IC

3. FIG 11 and Fig 12 shows SAT inspection under different mode on top and bottom of the package showed delamination between the interface of mould compound and paddle / lead surface. No delamination observed on the die surface.

A-Scan Mode: Delamination was found between the surface interface of moulding compound and lead finger

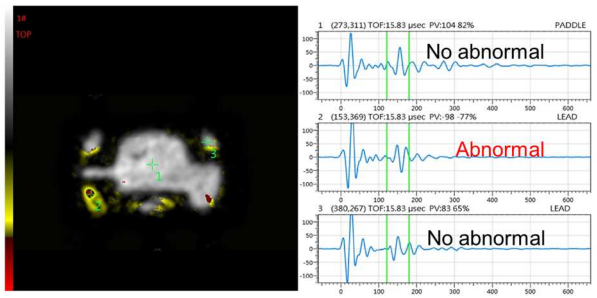

FIG 11 Top side: Scanning is focused on paddle and lead surface

A-Scan Mode: Delamination observed between the interface of mould compound and paddle / lead surface as shown in FIG 12

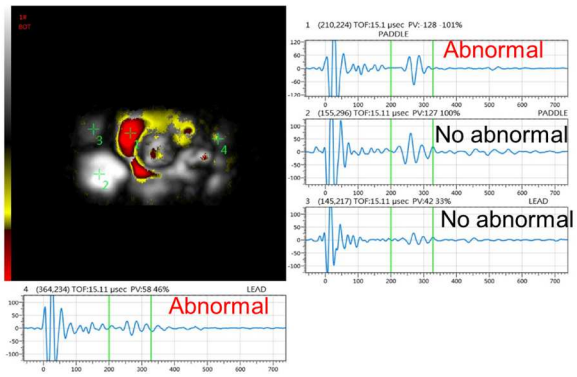

FIG 12 Bottom side: Scanning is focused on paddle and lead surface

4. Resistive I-V curve was observed on Pin 1 and 2 at ambient temperature. These pins have abnormal I-V curve at hot temperature testing. Please refer to detailed TABLE 1,2 and 3.

IV. Conclusions

V. Since 5G application is widely used, missing pulse would impact on timing and synchronization.

VI. The missing pulse failure nature is highly difficult to identify at customer application and would cause huge damage.

VII. This paper describes the mechanism to identify faulty OCXO and avoid the usage on 5G application. This analysis and work will bring good awareness in selection of components for 5G application.

VIII.

New mechanism is effective in detection of OCXO with faulty behavior as missing clock pulse at any instant of time and also used to define reliability of OCXO. This mechanism can detect malfunction of any component in an OCXO.

Different test conducted on Output Buffer IC from failed OCXO as listed below:

a) 2D X-ray inspection did not detect obvious wire anomaly on the sample.
b) SAT inspection under different mode on top and bottom of the package showed delamination between the interface of mould compound and paddle / lead surface. No delamination observed on the die surface.
c) Resistive I-V curve was observed on Pin 1 and 2 at ambient temperature. These pins also open I-V curve at hot temperature testing.
d) Delamination at pin 4 observed. Further inspection showed mould void at the right side of the tie bar near pin 5 which correlates with the delam observed during thru scan.

Based on the trails and analysis done on Buffer IC, confirmed the delamination and high resistance at PINs in one of the contribution for failure. Still there is scope for further analysis on Missing Pulse failure nature and other contributions.

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